

Claims

- [c1] 1. A method of multiple input multiple output system identification that utilizes dynamic construction of system response model and contains following steps:
recursive validation of the model accuracy on dynamically adjustable bands of allowable frequencies;
repetitive update of the model at dynamically selected bands of allowable frequencies.
- [c2] 2. A method of multiple input multiple output system identification that utilizes dynamic construction of system response model and contains following steps:
clustering analysis of the model during updates that identifies statistically significant changes in the model over specific bands of adjustable frequencies;
split of the model onto several models associated with individual clusters and invalidation of bands of allowable frequencies on which clustering was detected;
- [c3] 3. A method of multiple input multiple output system identification that utilizes dynamic refinement or revalidation of system response model and is invoked during normal operations of said system and said method con-

tains steps of claims 1 or 2.

[c4] 4. A method of multiple input multiple output system identification that utilizes dynamic construction of system response model and said model is accounting for possible hysteresis in the system and identification steps involve repetitive use of control inputs that shapes are defined as a functions with wide-band frequency spectrum and either infinitely piecewise smooth or having k piecewise continuous derivatives.

[c5] 5. A method of multiple input multiple output system identification that utilizes dynamic construction of system response model and said model is accounting for possible hysteresis in the system and uses method of claim 4 and said method contains steps of claims 1 or 2 or 3.

[c6] 6. A method of identification of multiple input multiple output system that dynamically constructs system model which incorporates input-input dependency and output-output dependency and at some state can be represented in matrix form as

$$\mathbf{g}(t) = \begin{bmatrix} \mathbf{g}_0 & (\mathbf{I} - \mathbf{g}_0)^{-1} \mathbf{g}_1 \\ (\mathbf{I} - \mathbf{g}_3)^{-1} \mathbf{g}_2 & \mathbf{g}_3 \end{bmatrix}$$

, where g_0 and g_3 are square matrixes.

- [c7] 7. A method of identification of a steady state among multiple possible steady states of multiple input multiple output system that invokes the model of the system according to claim 6 and includes step of matching vector of function or vector of time series to one of existing system response matrix, wherein said vector composed of inputs and outputs of the system and said matrix is structured according to claim 6 and matching process involves convolution or product of said matrix an vector.
- [c8] 8. A method of open-loop or close-loop feedback control of multiple input multiple output system that utilizes dynamically constructed or dynamically refined model that comprises plurality of linear models and wherein said linear models have identified associations with trajectory of changes of control inputs of said system and direction of following said trajectory, and wherein said dynamic construction or refinement is in accordance with claim 4.
- [c9] 9. A method of open-loop or close-loop feedback control of multiple input multiple output system that utilizes dynamically constructed optimal control solutions for control inputs of said system and wherein each said solution is created for specific steady state of the system

and for specific values of constraints imposed on the system and said control and said method includes following steps:

a priory creation of plurality of optimal solutions for control inputs;

real-time lookup of optimal solution based on current steady state of the system and closest match of current functions of inputs and outputs of said system to values of *a priory* selected constraints and where said lookup may be accelerated by means of *a priory* indexing or ordering of said constraints.

- [c10] 10. A digital algorithm implementing method of claim 1 that realized as high-level software language or low level binary code and aided for execution on two ore more digital processing devices.
- [c11] 11. A digital algorithm implementing method of claim 2 that realized as high-level software language or low level binary code and aided for execution on two ore more digital processing devices.
- [c12] 12. A digital algorithm implementing method of claim 4 that realized as high-level software language or low level binary code and aided for execution on two ore more digital processing devices.

- [c13] 13. A digital algorithm implementing method of claim 6 that realized as high-level software language or low level binary code and aided for execution on two ore more digital processing devices.
- [c14] 14. An digital algorithm implementing method of claim 7 that realized as high-level software language or low level binary code and aided for execution on two or more dig-ital processing devices.
- [c15] 15. An digital algorithm implementing method of claim 8 that realized as high-level software language or low level binary code and aided for execution on two or more dig-ital processing devices.
- [c16] 16. An digital algorithm implementing method of claim 9 that realized as high-level software language or low level binary code and aided for execution on two or more dig-ital processing devices.
- [c17] 17. [Claim Reference] [Claim Reference] [Claim Refer-ence] [Claim Reference] [Claim Reference] [Claim Refer-ence] [Claim Reference] [Claim Reference] [Claim Refer-ence]An apparatus incorporating only single digital pro-cessing device and at least one method of this invention and said apparatus operating as close-loop feedback controller only.

- [c18] 18. [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] An apparatus incorporating only single digital processing device and at least one method of this invention and said apparatus operating as open-loop or feed-forward controller only.
- [c19] 19. [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] An apparatus incorporating multiple single digital processing devices and at least one method of this invention and said apparatus operating as close-loop feedback controller only.
- [c20] 20. [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] [Claim Reference] An apparatus incorporating multiple single digital processing devices and at least one method of this invention and said apparatus operating as open-loop or feed-forward controller only.